## REMARKS

Claims 8-10 and 15-25 are pending and are unamended. Claims 1-7, 11-14, and 26-53 were previously canceled.

Accordingly, no new matter has been added.

### Entry of Rule 116 Response

Entry of this response is requested because this response does not raise any new issues that would require further consideration and/or search. No new claims are being presented in this response. No new matter is raised by this response. Lastly, it is requested that the response be entered even if the application is not allowed because this response will place the application in better form for appeal by materially simplifying the issues.

If the application is not in proper form for allowance, Applicants request that the Examiner telephone the undersigned to discuss any further outstanding issues.

### Request for Interview Prior to Formal Action on Response

Applicants request an interview prior to formal action on this response. An "Applicant Initiated Interview Request Form" accompanies this response. Please contact Applicants' undersigned representative to schedule the interview.

### 35 U.S.C. § 102(e) Prior Art Rejection

The Examiner has rejected claims 8-10 and 15-25 under 35 U.S.C. §102(e) as being anticipated by Applicant's Prior Art (Fig.2) (hereafter referred to as the APA). The Applicants respectfully traverse these rejections.

Applicants incorporate herein the arguments presented in the previous response. Additional arguments are presented below.

1. Patentability of independent claims 8 and 23 over the APA

Claims 8 and 23 recite (underlining added for emphasis):

8. An integrated circuit device receiving signals from a signal pad, comprising at least one substrate-biased silicon diode responsive to the signals from the signal pad for providing electrostatic discharge protection.

23. An integrated circuit device receiving signals from a signal pad, comprising:

a first plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals, each of the first plurality of substrate-biased silicon diodes including a p-portion and an n-portion;

a second plurality of serially coupled substrate-biased silicon diodes responsive to the signals from the signal pad for providing electrostatic discharge protection from the signals, each of the second plurality of substrate-biased silicon diodes including a p-portion and an n-portion; and

a detection circuit for detecting signals from the signal pad and providing a bias voltage to the first and second plurality of substrate-biased silicon diodes,

wherein the signal pad is coupled to the p-portion of one of the first plurality of substrate-biased silicon diodes and the n-portion of one of the second plurality of the substrate-biased silicon diodes.

a. APA depiction of diodes does not disclose or suggest a substrate-biased silicon diode (SBPD)[1]

The APA discloses a prior art structure designed to limit the destructive impact of electrostatic discharge (ESD) current on an integrated circuit (IC). See Figure 2 and page 2, lines 16-22 of the specification. To accomplish this protection, Figure 2 discloses the use of four diodes Dp1, Dn1, Dp2, and Dn2, a VDD-to-VSS ESD Clamp Circuit, and a grounded pad to channel ESD current to ground in a path that bypasses the internal circuits of the IC. See Figure 2 and page 2, lines 16-22 of the specification. The specification refers to this structure as a dual-diode structure and not as dual-SBPD structure. See page 2, line 17 of the specification. The specification does not identify the diodes Dp1, Dn1, Dp2, and Dn2 as substrate-biased silicon diodes (SBPDs). In addition, although the specification suggests that the diodes of the APA could be STI-bound diodes or polysilicon-bound diodes, the symbols used in Figure 2 (the APA) to depict Dp1, Dn1, Dp2, and Dn2 clearly indicate to those skilled in the art that those diodes are conventional diodes and not substrate-biased silicon diodes (SBPDs). See Figures 2 and 3, and page 3, lines 7-14 of the specification.

Further, the specification defines the circuit symbol for the SBPD of the present invention relative to the cross sectional view of the SBPD. See Figure 10 and page 19, lines 3-4 of the specification. The circuit symbol defined in Figure 10 for a SBPD is different from that of the symbol used in Figure 2 for Dp1, Dn1, Dp2, and Dn2. In addition, Figure 11 depicts a circuit diagram for an ESD protection circuit with dual-SBPD architecture. See Figure 11 and page 19, lines 4-12 of the specification. The ESD circuit protection diagram of Figure 11 looks substantially like the APA with the significant exception that the circuit symbol defined in Figure 10 is used to describe (in addition to the text identifiers) the diodes employed in Figure 11 as SBPDs. See Figures 10 and 11. The specification clearly distinguishes the prior art diodes Dp1, Dp2, Dn1, and Dn2 of the APA (Figure 2) as conventional diodes and the diodes SBPD1,

[1] In the specification, the acronym "SBPD" is used throughout to refer to both the embodiment of a substrate-biased silicon diode as well as a substrate-biased polysilicon diode. See Figures 4 and 6. Both embodiments are enabled by the specification and this paper will use "SBPD" to refer to both embodiments.

SBPD2, SBPD3, and SBPD4 as substrate-biased silicon diodes. See Figures 2 and 11, page 2, lines 16-22 of the specification, and page 19, lines 4-12 of the specification.

b. Examiner's combination of prior art diodes to anticipate SBPDs is improper

On page 2 of the Office Action, in the fourth paragraph, the Examiner refers to the combination of Dp1/Dn1 as depicted in the APA as equating to a substrate-biased silicon diode (SBPD). The Examiner further states that Dp1 is a p-type polysilicon portion of a SBPD and that Dn1 is an n-type polysilicon portion of a SBPD. Also, the Examiner states that the center polysilicon portion of Figure 1B prior art polysilicon-bound diode is disposed between Dp1 and Dn1, thereby anticipating a SBPD. The present invention does not suggest or disclose any such combination as the Examiner states to anticipate the use of SBPDs, or of serially coupled SBPDs, in the ESD current protection circuit of the APA.

None of the various embodiments of a substrate-biased silicon diode disclosed in the present invention suggest that a SBPD is a combination of two distinct conventional diodes with the further combination of the polysilicon center portion of Figure 1B. See Figures 4-7 and 10-11. In each of the embodiments disclosed in the present invention, a SBPD is a semiconductor layer of silicon (or polysilicon) with a center portion disposed between and contiguous with a p-doped portion and an n-doped portion. See Figures 4-6 and 10. Any diode disclosed or suggested by the APA is a complete semiconductor diode, each including its own P-N junction (a p-doped portion and an n-doped portion). The present invention does not suggest or disclose combining two separate diodes, each with their own P-N junction, and the addition of a center layer to create a SBPD.

c. Summary

In sum, the APA does not disclose or suggest the use of SBPDs in an ESD protection circuit. Also, the Examiner has improperly combined two distinct and separate prior art diodes disclosed in the APA and combined them with a center component of a prior art diode to find that

the APA anticipates the use of SBPDs. Accordingly, the Applicants respectfully request that the Examiner reconsider and withdraw the rejections to claims 8 and 23.

2. Patentability of dependent claims 9-10, 15-22, and 24-25 over the APA

Claims 9-10 and 15-22 depend from claim 8 and claims 24-25 depend from claim 23. Accordingly, they are believed to be patentable for at least the reason that they are dependent upon patentable base claims and because they recite additional patentable elements.

Therefore, the Applicants respectfully request that the Examiner reconsider and withdraw the rejections to claims 9-10, 15-22, and 24-25.

**Conclusion**

Insofar as the Examiner's rejections were fully addressed, the instant application is in condition for allowance. Withdrawal of the Final Rejection, entry of this response, and issuance of a Notice of Allowability of all pending claims is therefore earnestly solicited.

Respectfully submitted,

CHYH-YIH CHANG et al.

NOV. 21, 2006 By: Clark Jablon
(Date)

CLARK A. JABLON
Registration No. 35,039
AKIN GUMP STRAUSS HAUER & FELD LLP
One Commerce Square
2005 Market Street - Suite 2200
Philadelphia, PA 19103-7086
Telephone: (215) 965-1200
Direct Dial: (215) 965-1293
Facsimile: (215) 965-1210
E-Mail: cjablon@akingump.com

CAJ/MJ